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| Form PTO-1449 (Modified) IDS INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary) 02/20/01 | | | | Atty. Docket No. 1662-25000 (P00-3078) | | Serial No. 09/740,419 | |
| | | | | Applicants Andre C. SEZNEC et al. | | | |
| | | | | Filing Date December 19, 2000 | | Group UNKNOWN | |



| REFERENCE DESIGNATION U.S. PATENT DOCUMENTS | | | | | | | |
|---|--|-----------------|------|--|-------|-----------|----------------------------|
| EXAMINER INITIAL | | DOCUMENT NUMBER | DATE | | CLASS | SUB-CLASS | FILING DATE IF APPROPRIATE |
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| FOREIGN PATENT DOCUMENTS | | | | | | | |
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| | | DOCUMENT NUMBER | DATE | COUNTRY | CLASS | SUB-CLASS | Translation YES NO |
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| OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.) | | |
|--|----|--|
| h | AA | Multiple-Block Ahead Branch Predictors, A. Seznec et al., ASPLOS VII 10/96 MA, USA, 1996 ACM 0-89791-767-7/96/0010, Pages 116-127 |
| h | AB | Trace Cache: a Low Latency Approach to High Bandwidth Instruction Fetching, E. Rotenberg et al., 1072-4451/96 1996 IEEE, Pages 24-34 |
| h | AC | Increasing the Instruction Fetch Rate via Multiple Branch Prediction and a Branch Address Cache, T. Yeh et al., 1993 ACM 0-89791-600-X/93/0007/0067, Pages 67-76 |
| h | AD | Multiple Branch and Block Prediction, S. Wallace et al., 1997 IEEE, Proceedings of the Third International Symposium on High Performance Computer Architecture, February 1-5, 1997, Pages 1-10, plus cover sheet |
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| EXAMINER [Signature] | DATE CONSIDERED [Signature] |
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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP §609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.

D.P.
07/26/04

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